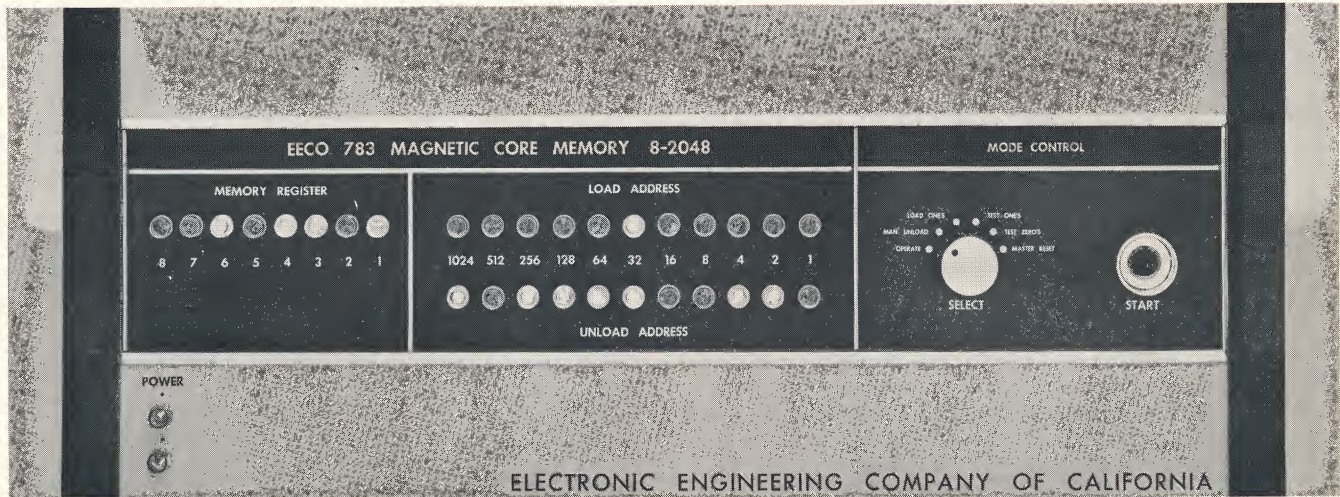




DATA
SHEET

EECO MAGNETIC CORE MEMORIES

EECO 781	Random Access
EECO 782	Sequential Access
EECO 783	Sequential Interlace



- Self-check with visual indicators.
- 200 kc, 5 microsecond full cycle time.
- Automatic data restore on unload.
- Manual unload for system check.
- Noise rejection input circuits.

Character Capacity.....256 to 4096
Bits per Character.....2 to 8

GENERAL

EECO 781 RANDOM ACCESS

This memory permits data to be loaded or unloaded, one character at a time, into or from any address in the memory. A load or unload and an address command are required for each operation. Data is accepted by the memory at a constant or intermittent rate and is unloaded, upon command, in any desired character order either in blocks or in a continuous stream.

Address commands, supplied by external equipment, are dc level shifts on multiple lines. Both the address and its complement are required (20 lines are used for a 1024-bit capacity memory).

The random access memory is used in data processing systems which require some rearranging and formatting of data.

EECO 782 SEQUENTIAL ACCESS

This memory is essentially a random access memory with one address counter. The counter permits characters to be loaded serially in blocks and unloaded in the same sequence (first in, first out).

Load and unload commands are supplied by external equipment. A counter reset command is required to reset the address counter after each complete load or unload cycle. Loading and unloading can be either at a clocked or asynchronous rate.

The sequential access memory is used for storing and reading out blocks of data where it is possible to stop loading while the stored data is read out.

As an example, this type of memory can be used in a paper-tape-to-magnetic-tape converter where the paper tape reader fills the memory and then stops. Upon receipt of an unload command, the data is read out onto the magnetic tape. The magnetic tape unit is then stopped and a new block of data is received from the paper tape reader.

EECO 783 SEQUENTIAL INTERLACE

The sequential interlace memory has two internal address counters; one controlling loading, the other controlling unloading. Each counter advances one count after a character is received or read out causing the memory to unload characters in the same sequence as they are loaded.

External load and unload commands control the memory sequencing. Data storing and read out may be performed sequentially in blocks or loading and unloading cycles may be interlaced. This interlacing permits blocks of characters to be loading and unloading simultaneously provided 5 microseconds are allowed between each load and unload cycle.

The maximum speed of loading or unloading with the load and unload data interlaced is 100 kc for load and 100 kc for unload. If the unload is operating at 100 kc with data gaps, the incoming rate must be controlled to ensure that data is not loaded into an address which has not been read out.

A typical application is one in which the memory is used as a converter for buffering the output of an analog-to-digital converter to a magnetic tape record in computer format.

In this case, the A/D converter may continually load the memory at a clocked or an asynchronous rate. When a block of data is accumulated in the memory, it is read out at a clocked rate and then stopped in order to provide a data gap on the computer tape. Five microseconds must separate an incoming character from an output character.

The memory provides a dc level signal to designate whether it is loading or unloading. This can be used as an external command to interlace incoming characters between the output characters.

CHARACTERISTICS

SELF CHECK (EECO 782 & 783 ONLY)

Two self-check modes are available. In the "test one" mode, binary "ones" are recirculated through the core storage at a 200-kc rate to test for errors. In the "test zero" mode, binary "zeros" are recirculated. If an error occurs in either mode, the recirculation automatically stops and the front panel indicators display the error and its address.

MANUAL UNLOAD AND LOAD ONES

These modes are primarily for use in checking equipment external to the memory.

In the "manual unload" mode, one character in the memory is unloaded each time the MODE START push button is pressed. The front panel memory register displays the character and the front panel address indicators show the address being read. The address counter advances one position for each unload operation. The character remains in the original position in the memory after readout.

The "load ones" mode permits the entire memory

to be loaded with binary "ones" by setting the MODE SELECT switch to LOAD ONES and pressing the MODE START push button.

DATA INPUT CIRCUITS

NOR circuits are used for input gates. These gates require that the dc level be held for at least 2.5 μ sec. Sharp noise spikes on the incoming data lines do not affect the memory as long as the data signal remains within the dc level limits.

Input data level can vary over a wide range from -6 volts to -18 volts for a binary "zero." Binary "one" input can vary between 0 V dc and ± 25 V dc.

MEMORY REGISTER

The memory register accepts both load and unload data upon command. NOR latches are used in the register.

AUTOMATICALLY RESTORED READOUT

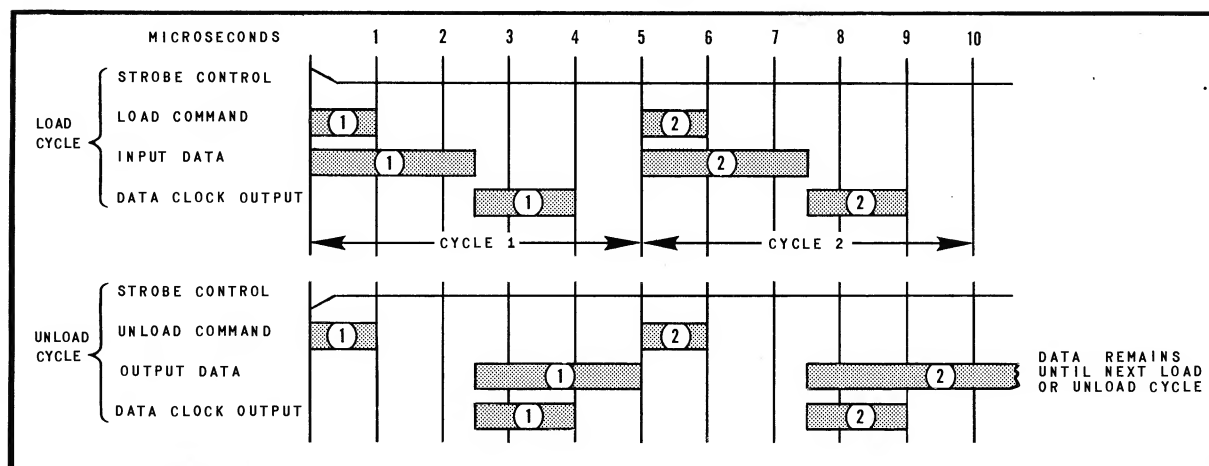
Unloaded data is recirculated so that it remains in the memory after readout. Incoming data commands automatically clears the selected word.

SPECIFICATIONS

CAPACITY	256, 512, 1024, 2048, and 4096 characters, each containing from 2 to 8 bits.	Duration	1.5 μ sec occurring 2.5 μ sec after load or unload command.
OPERATING MODE	Character bits loaded or unloaded in parallel. Characters loaded or unloaded individually or in blocks.	Loading	8.2 K ohms minimum resistance to ground.
SPEED	200 kc, 5 μ sec per cycle. A cycle is a load or unload operation. Load and/or unload commands must be separated by at least 5 μ sec.	STROBE CONTROL OUTPUT	Dc level distinguishing load and unload cycles.
INPUT CONTROL SIGNALS	"Load," "unload," "reset load counter," "reset unload counter," "master reset," "Master reset" pulse rate must be less than 2,000 per second.	Level during "load"	-10 V dc \pm 1 V.
Amplitude	Positive-going pulse or level shift of nominal 8-volts amplitude (5-volt minimum, 11-volt maximum). AC coupled.	Level during "unload"	0 V dc \pm 0.25 V.
Rise Time	0.5 μ sec maximum. Minimum pulse width is 1 μ sec. At 200-kc input repetition rate, maximum pulse width is 3 μ sec.	Loading	8.2 K ohms minimum resistance to ground.
Noise Rejection	Up to 3 volts peak-to-peak noise rejection.	OPERATING CONTROLS	MODE SELECT (OPERATE, MANUAL UNLOAD, LOAD ONES, TEST ONES, TEST ZEROS, MASTER RESET), and MODE START.
Input Impedance	250 pf to ground.	INDICATORS	Indicators for each level of memory register and for each bit position in address counters; dc power indicators verify power-on condition for both +12 V dc and -12 V dc individually.
INPUT DATA SIGNALS	Dc levels on 2 to 8 parallel lines (single-ended input).	SELF-CHECK MODES	Either all binary "zeros" or all binary "ones" are set into memory. Characters are then tested sequentially in a non-destructive unload operation at a rate of 200,000 cycles per second. If error is detected, address counters stop and address of error is indicated; otherwise, test continues until manually stopped.
Binary "One"	0 V dc \pm 0.25 V (ground).	TEST MODE	
Binary "Zero"	-12 V dc \pm 6 V.	Manual Unload	Pressing the MODE START push button unloads one character from the memory. Address advances one position each time the push button is pressed.
Input Impedance	8.2 K ohms to ground.		Character readout and location are displayed in the memory register display and unload address display on the front panel.
Noise Rejection	Not affected by spikes as long as dc levels are within the tolerance limits. Input gates are closed except for the first 2.5 μ s of a load cycle.		Readout is non-destructive.
Input signal timing	Data levels must be stabilized within voltage limits at the time of the load command and require a duration of at least 2.5 μ sec.	Load Ones	Pressing the MODE START push button loads the entire memory with "ones."
OUTPUT DATA SIGNALS	Dc levels on 4 to 16 parallel lines; output levels occur 2.5 μ sec maximum (double-ended outputs) after unload pulse and remain until occurrence of next load or unload pulse.	Master Reset	When the MODE START push button is pressed, the entire memory and the memory registers are cleared—i.e., set to "zeros."
Binary "One"	True and complement 0 V dc \pm 0.25 V and -10 V dc \pm 1 V.	POWER REQUIREMENTS	117 V ac \pm 10%, 57 to 420 cps, 1 phase, 1.25 amperes, 146 watts.
Binary "Zero"	True and complement -10 V dc \pm 1 V and 0 V dc \pm 2.5 V.	DIMENSIONS	19 inches wide x 7 inches high x 19 inches deep, excluding the mating plugs. Chassis sides are drilled for Chassis-Trak CTD-120 sliders.
Rise Time	No greater than 0.5 μ sec.	WEIGHT	45 lbs.
Loading	Minimum load resistance 1000 ohms to ground.	ENVIRONMENTAL CONDITIONS	
ADDRESS LEVEL OUTPUTS	Dc levels indicating load and unload addresses in parallel form (single-ended).	Ambient Temperature	
Binary "One"	0 V dc \pm 0.25 V.	Operating	0°C to +50°C (32°F to +122°F).
Binary "Zero"	-6.5 V dc \pm 0.5 V.	Non-Operating	-30°C to +85°C (-22°F to +185°F).
Loading	8.2 K ohms minimum resistance to ground.	Relative Humidity	0 to 95%.
DATA CLOCK OUTPUT	Positive-going direct-coupled pulse, allows clocking of external circuits from memory.	CONNECTORS	
Quiescent Level	-12 V dc \pm 1 V.	Data	J1—Winchester XAC50PF2A006* P1—Winchester XAC50SD3A300 J2—Winchester XAC50PF2B006 P2—Winchester XAC50SD3B300
Active Level	0 V dc \pm 0.5 V.		
Rise Time	0.25 μ sec maximum.		

*8-2048 Sequential Interlace Memory use Amp 50 pin connectors

TIMING DIAGRAM



DATA HANDLING EQUIPMENT

Model	Equipment Name and Description
EECO 751	Format Control Buffer. Converts analog or digital data to computer format. Writes a magnetic tape ready for computer use. IBM, Univac, RCA & other formats available.
EECO 754	Magnetic Tape Adapter. Provides for reading and writing GE ERMA and GE 210 magnetic tapes from IBM 1401 computer.
EECO 760	Analog-to-Digital Converter. 12-bit, 40 KC sample rate.
EECO 780	Shaft Angle Translator. Converts output from optical shaft angle encoder to degrees of angle. Both visual display and BCD outputs available.
EECO 790	Datachron Computer Time Clock. Accurately logs computer time. Plug in connection to IBM 1401, 1410, 7070, etc.
EECO 795	Computer Paper Tape Reader. Inexpensive plug-in paper tape reader for IBM 1401 computer.



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